Claims

[c1] 1. A wafer level packaging process, comprising the steps of:
providing a wafer having a plurality of chips thereon, wherein the wafer has an active side;
forming an insulation layer over the active side of the wafer, wherein the insulation layer exposes a surface;
forming a plurality of open windows in the insulation layer, wherein each open windows passes through the insulation layer;
forming a plurality of conductive paste plugs, wherein each of the conductive paste plugs is in the respective open window ;
forming a metallic layer over the insulation layer;
patterning the metallic layer to form a plurality of ball pads electrically connected with the conductive paste;
forming a solder mask over the insulation layer surface to expose the ball pads;
mounting a plurality of solder balls, wherein each of the solder balls is attached to the respective ball pad; and
dicing up the silicon wafer and the insulation layer to form a plurality of chip packages.

[c2] 2. The wafer level packaging process of claim 1, wherein the step of forming the insulation layer on the active side of the wafer includes spin-coating.

[c3] 3. The wafer level packaging process of claim 1, wherein the step of forming the insulation layer on the active side of the wafer includes laminating.

[c4] 4. The wafer level packaging process of claim 1, wherein the step of forming open windows in the insulating layer includes conducting photolithographic and etching processes.

[c5] 5. The wafer level packaging process of claim 1, wherein the step of forming open windows in the insulating layer includes laser drilling.

[c6] 6. The wafer level packaging process of claim 1, wherein the step of patterning the metallic layer to form the ball pads includes conducting photolithographic and etching processes.

[c7] 7. The wafer level packaging process of claim 1, wherein the wafer further includes a plurality of bumps on the active side of the wafer, wherein each of the bumps is formed inside the respective open window of the insulation layer.

[c8] 8. The wafer level packaging process of claim 1, wherein before the step of forming the insulation layer on the active side of the wafer, further includes forming a redistribution circuit layer on the active side of the wafer.

[c9] 9. A process of forming an insulation layer having a plurality of conductive paste plugs therein over a wafer, comprising the steps of:
providing a wafer having a plurality of chips therein, wherein the wafer has an active side;
forming an insulation layer over the active side of the wafer;
forming a plurality of open windows in the insulation layer; and
forming a plurality of conductive paste plugs, wherein each of the conductive paste plug is inside the respective open window.

[c10] 10. The process of claim 9, wherein the step of forming the insulation layer on the active side of the wafer includes spin-coating.

[c11] 11. The process of claim 9, wherein the step of forming the insulation layer on the active side of the wafer includes laminating.

[c12] 12. The process of claim 9, wherein the step of forming open windows in the insulation layer includes conducting photolithographic and etching processes.

[c13] 13. The process of claim 9, wherein the step of forming open windows in the insulation layer includes laser drilling.

[c14] 14. The process of claim 9, wherein the wafer further includes a plurality of bumps on the active side of the wafer, wherein each of the bumps is inside the respective open window of the insulation layer.

[c15] 15. The process of claim 9, wherein before the step of forming the insulation layer on the active side of the wafer, further includes forming a redistribution circuit layer on the active side of the wafer.

[c16] 16. A chip package structure, comprising:
a chip having an active side;
an insulation layer on the active side of the chip, wherein the insulation layer has a plurality of open windows that pass through the insulation layer;
a plurality of conductive paste plugs, wherein each of the conductive paste plugs is formed in the respective open window;
a patterned metallic layer with a plurality of ball pads on the insulation layer, wherein the ball pads are electrically connected to the conductive paste plugs;
a solder mask over the insulation layer to expose the ball pads; and
a plurality of solder balls, wherein each of the solder balls is mounted to the respective ball pad.

[c17] 17. The chip package structure of claim 16, wherein the structure further includes a redistribution circuit layer between the insulation layer and the chip, wherein the redistribution circuit layer comprises an insulation layer and a plurality of metallic circuit lines which criss-cross inside the insulation layer and connect electrically with the conductive paste plugs and the chip.

[c18] 18. The chip package structure of claim 16, wherein the structure also includes a plurality of bumps enclosed inside the open windows and connect electrically with the conductive paste plugs.

[c19] 19. An insulation structure having at least one conductive paste plug therein to be installed inside a chip package structure, comprising:
an insulation layer on the active side of a chip, wherein the insulation layer has at least one open window; and
conductive paste that completely filling the open window.

[c20] 20. The insulation structure of claim 19, wherein the structure further includes at least one bump inside the open window to connect electrically with the conductive paste.